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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/801,260	03/15/2004	Ichiro Fujimori	13912US04	2251

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EXAMINER	
CAO, PHAT X	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 08/11/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/801,260	FUJIMORI, ICHIRO	
	Examiner	Art Unit	
	Phat X. Cao	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-15 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-15 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 3-10 and 15 are objected to because of the following informalities:

- in claims 3-7, lines 1-2, "a second transistor type" should be changed to "said second transistor type";

- in claims 8-10, lines 1-2, "a first transistor type" should be changed to "said first transistor type";

- in claim 15, line 1, "said second noisy voltage source" should be changed to "a second noisy voltage source".

Appropriate correction is required.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 1-15 rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-10 of copending application No. 10/294,880. Although the conflicting claims are not identical, they are not patentably

distinct from each other because : both applications claim a system for reducing noise in a chip comprising a transistor of a first transistor type disposed within a transistor layer (or a second well), the transistor layer (or a second well) is shielded from the substrate layer by a shielding layer (or a first well) (also see claim 10). Moreover, the claims in the instant application are either broader versions of the claims in copending application 10/294,880 or are obvious variations thereof. Eventhough claim 1, for example of the instant application does not use exactly the same word, for example, "a transistor layer integrated within the chip, which is shielded from the substrate layer by a shielding layer", and the copending application recites "a second well disposed within the first well (claim 1)", "the first well is adapted to shield the substrate from noise emanating from a voltage source coupled to at least one of the first transistor ... (claim 10)", that shows no different meaning between these two elements. The facts are that the claims of the copending application have claimed the same goal and are not distinguished from each other.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical

Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

5. Claims 1-7, 9-10 and 12 are rejected under 35 U.S.C. 102(e) as being anticipated by McCormack et al (US. 6,395,591).

Regarding claims 1, 9 and 12, McCormack (Fig. 2) discloses a system for reducing noise in a chip, the system comprising: a substrate layer 10 integrated within the chip; a transistor layer 18/22/16 integrated within the chip, which is isolated or shielded from the substrate layer 10 by a shielding layer 12; at least one transistor of a first transistor type 29 that couples the transistor layer 18 to the shielding layer 12; and a quiet voltage source 26 (column 3, lines 50-55) that is coupled to the at least one transistor of the first transistor type; wherein the at least one transistor of the first transistor type 29 is disposed within the transistor layer 18, and wherein the shielding layer 12 is disposed between the substrate layer 10 and the transistor layer 18.

Regarding claims 2-5, McCormack further discloses: at least one transistor of a second transistor type 28 coupled to the shielding layer 12; wherein the at least one transistor of the second transistor type 28 is a N-type transistor, is disposed within the transistor layer 16, and is resistivity coupled to the P type shielding layer by the P type transistor layer 16.

Regarding claims 6-7, McCormack further discloses a first noisy voltage source or a digital voltage source 24 (column 3, lines 53-55) is coupled to a source of the at least one transistor of the second transistor type 28.

Regarding claim 10, McCormack further discloses the transistor of the first transistor layer having N type source/drain region, which is capacitively coupled to the P type-shielding layer.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over McCormack et al (US. 6,395,591) in view of Vinal (US. 5,151,759).

As discussed above, McCormack discloses the first transistor 29 being a NMOS, but not a PMOS.

However, Vinal teaches the converting of a NMOS transistor to a PMOS transistor by exchanging N for P and P for N (column 34, lines 41-47). Accordingly, it would have been obvious to convert the first transistor 29 form a NMOS to a PMOS because as taught by Vinal, the NMOS transistor device is analogous to the PMOS transistor device, with the device operational polarity and doping types reversed.

8. Claims 11 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over McCormack et al (US. 6,395,591) in view of Wei (US. 6,403,992).

McCormack discloses the shielding layer 12 is deep P-well, but not N-well which is capacitively coupled to the substrate layer 10.

However, Wei teaches the conventional of forming a transistor within a shielding layer of P-well, which is capacitively coupled to the N type substrate (Fig. 3), or a transistor within a shielding layer of N-well which is capacitively coupled to the P type substrate (Fig. 4). Accordingly, it would have been obvious to form the shielding layer 12 of McCormack with either N type or P type because they both provide the benefits of eliminating substrate effect, as taught by Wei (column 1, lines 47-60).

9. Claims 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over McCormack et al in view of Puar et al (US. 6,356,497).

McCormack does not disclose a noisy voltage source coupled to a source of the first transistor 29.

However, Puar (Fig. 5) teach a system for reducing noise in a chip by connecting a noisy voltage source 38 to a source of the transistor and a quiet voltage source VDD to a body (N+) of the transistor (column 4, lines 59-65). Accordingly, it would have been obvious to connect the source of the first transistor 29 of McCormack to a noisy voltage source (i.e., external devices) in order to receive/transmit the data from the transistor to the external devices.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phat X. Cao whose telephone number is (571) 272-1703. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PC
August 5, 2004

PHAT X. CAO
PRIMARY EXAMINER